Guidelines for Mask Design

1. Basic Fabricating Process (Conductor and Resistor) 2
   1.1. Mask Type: 2
   1.2. Mask Plate Size: 2
   1.3. Substrate and Design Size: 2
   1.4. Mask Sequence: 2
      1.4.1. Regular Etch Back Process 2
      1.4.2. Pattern Plate Process 3
   1.5. Gold Thickness and Etch Factor of Circuit Design: 7
   1.6. Resistor Length and Width: 7
   1.7. Laser Drill Alignment Target: 8
   1.8. Conductor – Resistor Alignment Target: 9
2. Special Process – Polyimide Process 9
   2.1. Process type 9
   2.2. Mask Sequence: 10
   2.3. Polyimide Etch Factor 11
   2.4. Polyimide Alignment Target 11
   2.5. Top Metal Alignment Target 12
   2.6. Top Metal Contact Alignment Target (STILL UNDER DEVELOPMENT) 12
3. Cutting Targets: 12
4. Step and repeat spacing: 15
5. Laser drilled hole targets: 15
6. Front to back alignment target 16
7. Fused Silica Substrate Exception 18

1. Basic Fabricating Process (Conductor and Resistor)

There are two different processes that we use to fabricate the circuits. They are Etch Back process and Pattern Plate process. The masks ordered are different for the two processes; one is the opposite of the other one. An extra mask is also required when we fabricate substrates using the pattern plate process, called **flash** mask.

The circuit boards are ceramic with overlays of tantalum-nitride (if applicable), Titanium-Tungsten and then gold. The circuits consist of gold conductors, while the resistors are made of tantalum. The field is the ceramic area of the final boards.

1.1. Mask Type:

Chrome on glass.

1.2. Mask Plate Size:

4.00” Square for 1” x 1”, 2” x 2” and 3.25” x 3.25” Substrate

5.00” Square for 4.00” x 4.00” Substrate

1.3. Substrate and Design Size:

The standard substrate sizes are 1.00” Square, 2.00” Square and 3.25” Square.

The mask should leave 1.27 mm (0.050”) minimum border on all 4 sides (Edge of circuit to edge of substrate)

1.4. Mask Sequence:

1.4.1. Regular Etch Back Process

1.4.1.1. The circuit mask will be a **positive** image or a **clear** field mask. The mask will be named **C1** for CONDUCTOR 1 (front side) and if required, **C2** for CONDUCTOR 2 (back side).

The **opaque** areas will be:

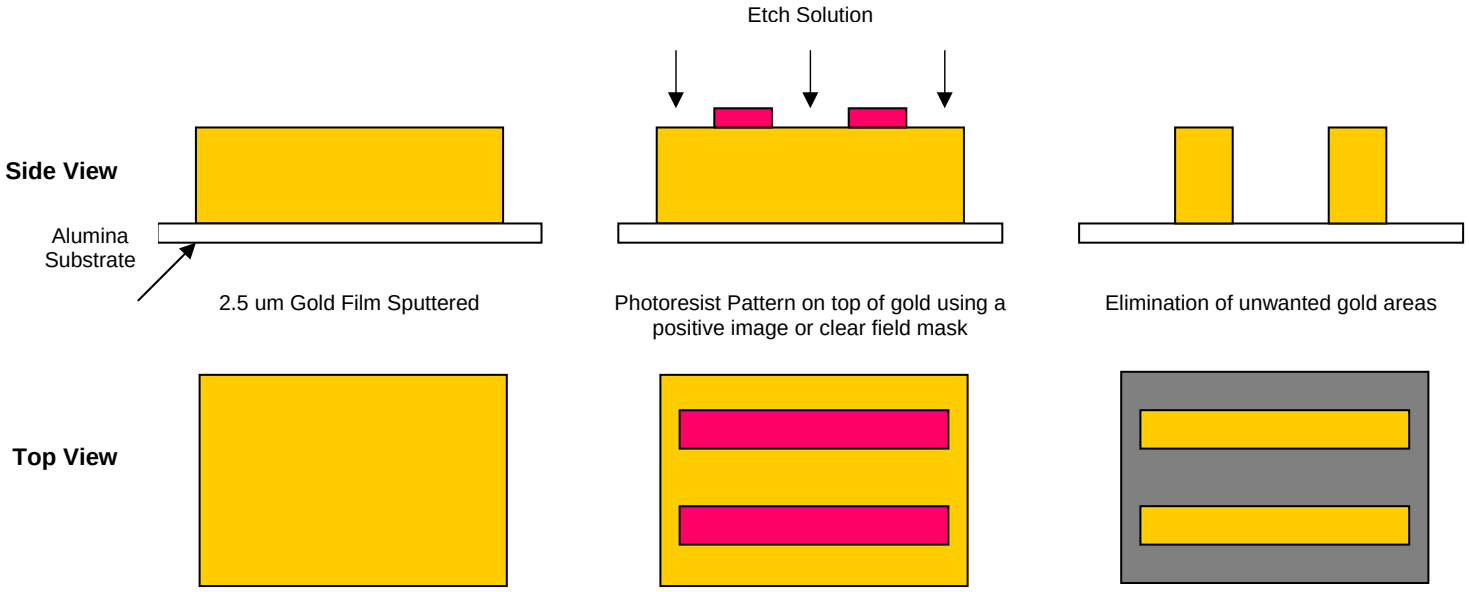
a) The circuit traces

b) The substrate alignment marks (when applicable)

c) The resistor alignment targets

d) The cutting targets

We are using positive photoresist that is made soluble by exposure to ultraviolet light. Any area that is covered by the opaque part of the mask will not be etched away, and areas that are clear on the mask will be etched when using the regular Etch Back process. Therefore, the mask is positive with respect to the final circuit. The opaque traces on the mask will produce circuit traces. It is easier to think this process as an elimination process. We eliminate any areas that are not needed.

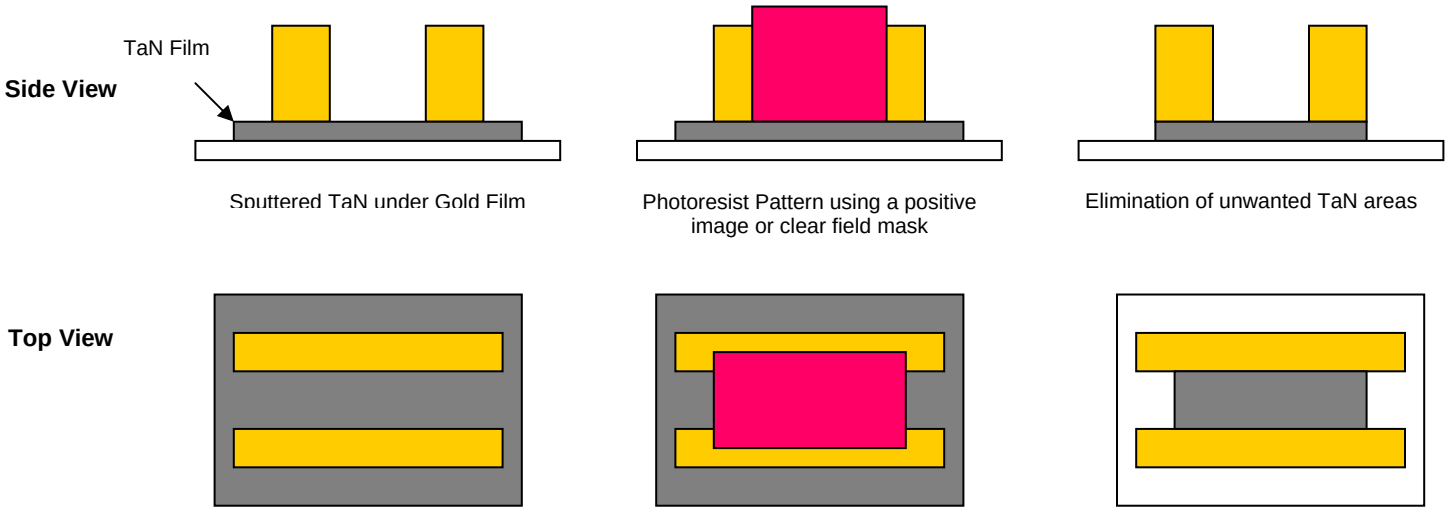


1.4.1.2. The resistor mask –R1 for front side (-R2 for backside if required) will be a **positive** image or a **clear** field mask.

The **opaque** areas will be:

a) The resistors

b) The resistors alignment targets



1.4.2. Pattern Plate Process

1.4.2.1. The circuit mask will be a **negative** image or a **dark** field mask. The mask will be named **PP1** for CONDUCTOR 1 (front side) and if required, **PP2** for CONDUCTOR 2 (back side). * **SEE DARK FIELD MASK NOTE**

The **open** areas will be:

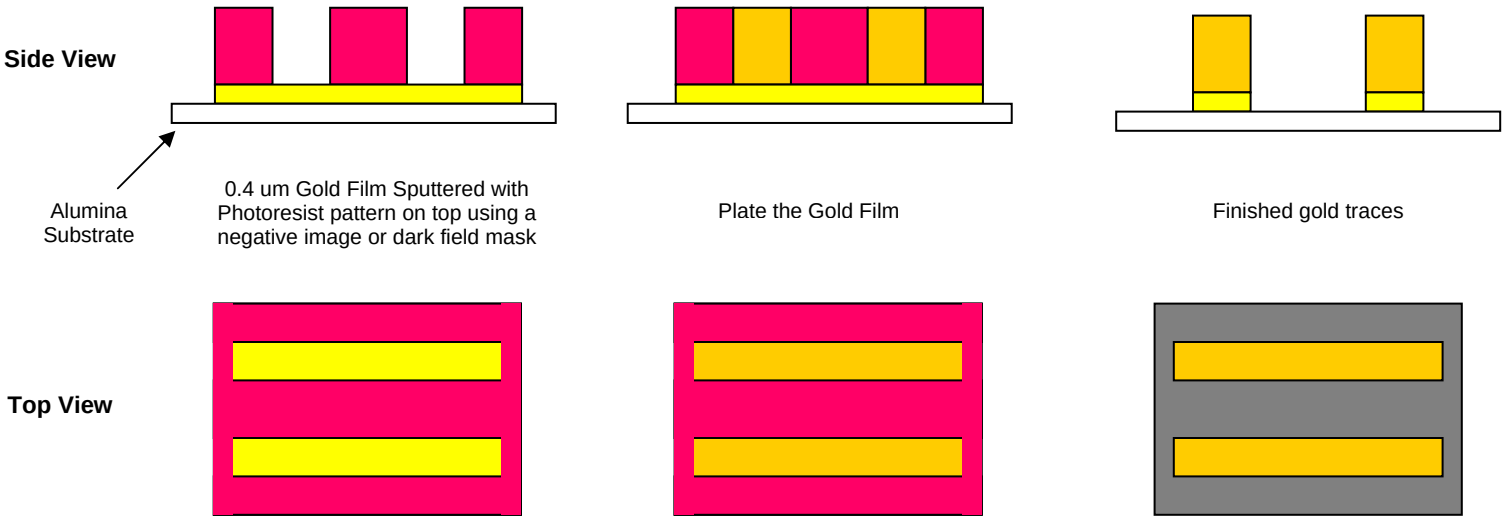
a) The circuit traces

b) The substrate alignment marks (when applicable)

c) The resistor alignment targets

d) The cutting targets

Positive photoresist is used for both etch back and pattern plate process. However, pattern plate process works in the opposite way of regular etch back process. We will plate gold on any open / uncovered area of the mask. The open areas on the mask will produce circuit traces. It is easier to think this process as a building process. We build gold in areas that are needed.



1.4.2.2. The flash mask – **F1** will be a **negative** image or a **dark** field mask. The flash mask F1 will align to the front side. No flash mask required for the back side.

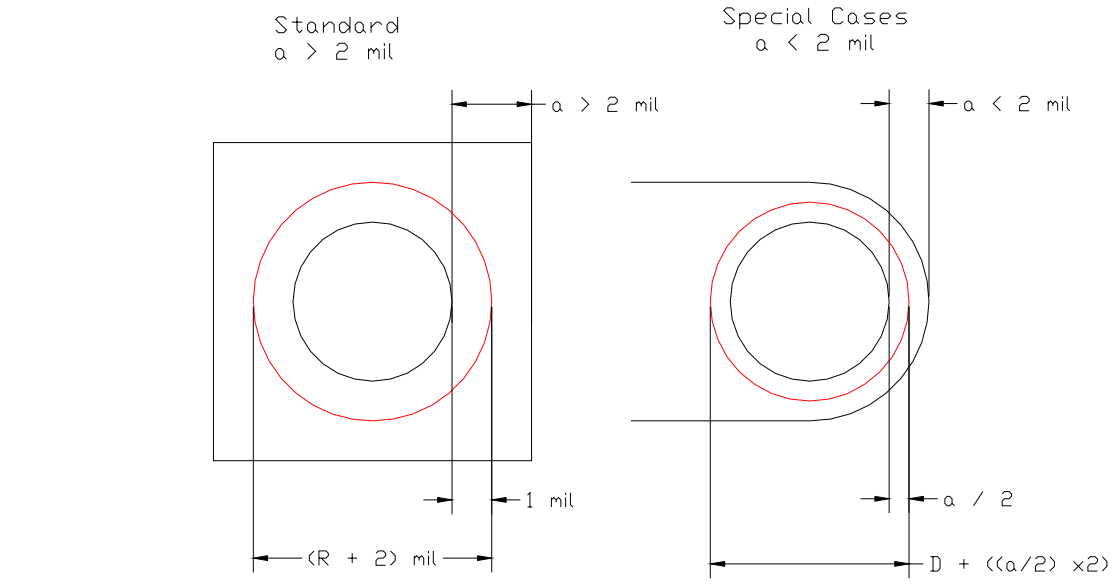
* **SEE DARK FIELD MASK NOTE**

The **open** areas will be:

a) The via holes. In general, the open via holes' diameter should be 2 mil larger than its design, x = (D + 2) in mil. In special case, where the edge the gold pad pattern around the hole is located less than 1 mil from the edge of the hole, then the open via holes' diameter should be

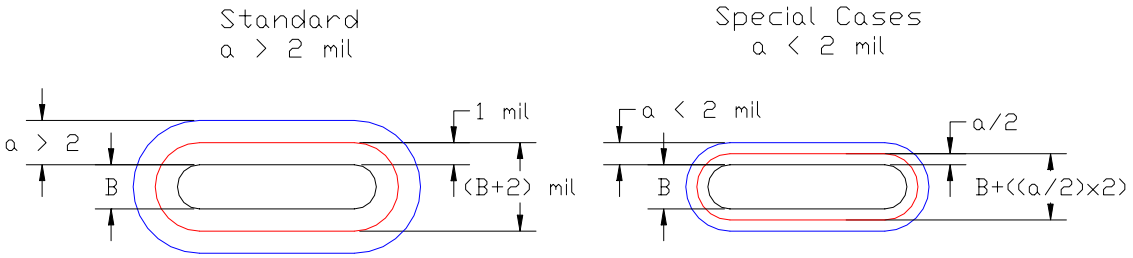
$$x = D + \left(\frac{a}{2} x 2 \right)$$

Where a is the distance between the edge of the hole to the edge of the gold pad.

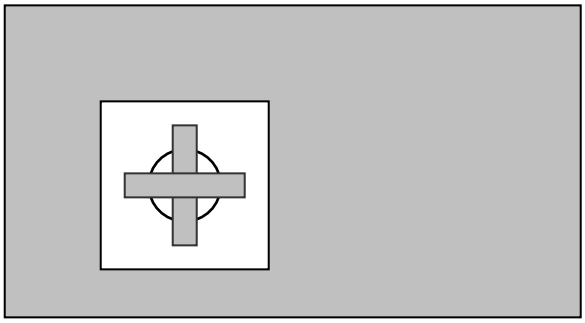


b) The slots that need a connection front to back or wrap around. The open area for slot should be larger than its design by 1 mil in each side, in standard case. However, in special case where the distance between the edge of the slot to the edge of the gold pad less than 1 mil, then the compensation should be:

$$x = B + \left(\frac{a}{2} x 2\right)$$



c) The laser drill target / alignment marks for any dark field mask or F1 mask. It has to be put in the middle of an open box to allow viewing of the substrate when aligning.



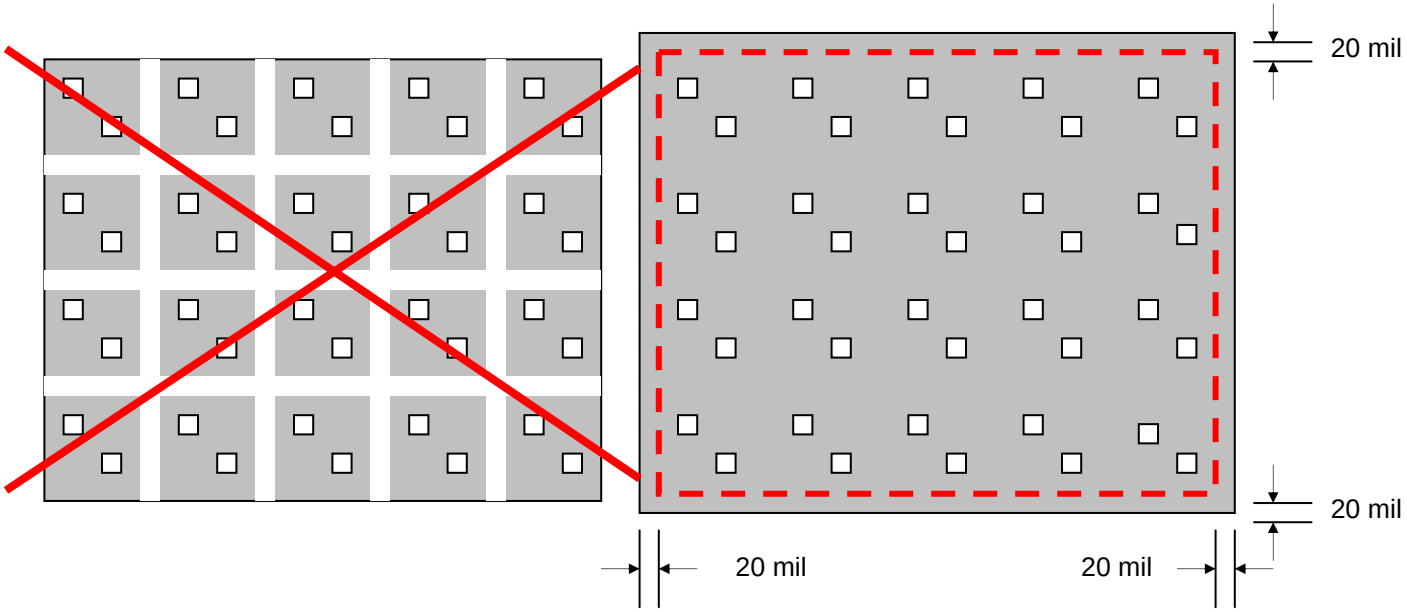
1.4.2.3. The resistor mask –**R1** for front side (-**R2** for back side if required) will be a **positive** image or a **clear** field mask.

The **opaque** areas will be:

a) The resistors

b) The resistors alignment targets

**DARK FIELD MASK NOTES



- **No** street line between circuits on **dark field**
- **Extend** another **20-mil** on all four sides of the dark field area for handling purpose. The broken lines show the real edge of the circuits.

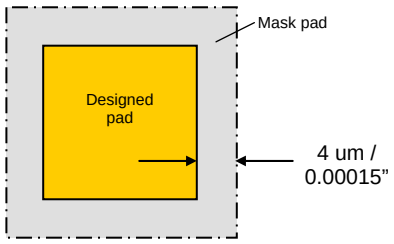
1.5. Gold Thickness and Etch Factor of Circuit Design:

The final standard gold thickness is 2.54 – 3.302 μm (.0001" -. 00013").

Different etch factor should also be applied for the two different processes. Etch factor have to be applied to all design pattern with **NO** exception. The following table shows both of the etch factor.

Type of process	Etch Factor
Etch back	**+** 8 μm / 0.0003" / 0.3 mil
Pattern Plate	**-** 1.3 μm / 0.00005" / 0.05 mil

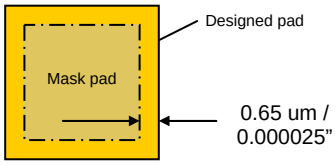
Be careful with the difference sign of the etch factor. The following diagram will help explain the difference.



ETCH BACK

+ 8 um / 0.0003"

Mask pad is **LARGER** than the designed pad



PATTERN PLATE

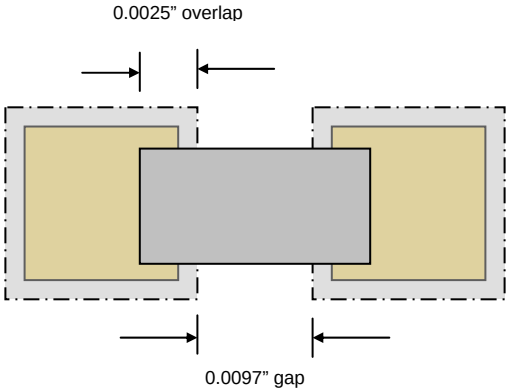
- 1.3 um / 0.00005"

Mask pad is **SMALLER** than the designed pad

1.6. Resistor Length and Width:

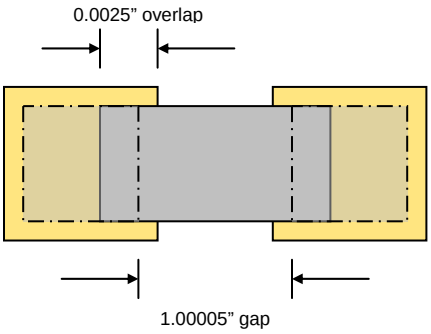
The length is determined by the gap made in the circuit mask. It is made narrower by one etch factor if etch back process is used. For example, if a .010" Gap of resistor length is required, the conductor mask should have a .0097" gap. If pattern plate process is used, then the conductor mask should have a 1.00005" gap. The resistor mask itself should have a .0025" overlap on each end of each resistor to assure proper alignment with the circuit mask.

0.010" Gap ideally



ETCH BACK

PATTERN PLATE



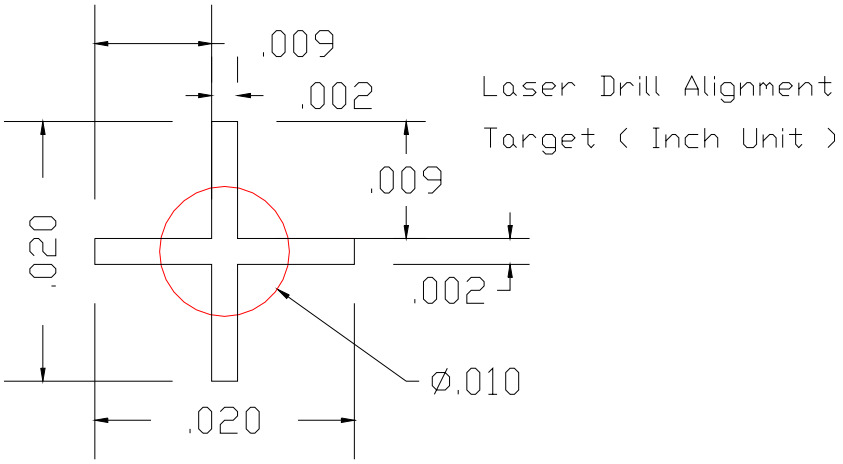
1.7. Laser Drill Alignment Target:

1.7.1. Diagram below represents out standard 0.010” laser drill alignment target.

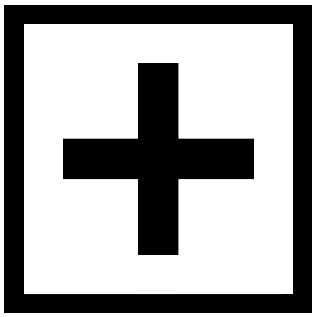
1.7.2. For more precise alignment, smaller laser drill alignment target can be used. MTC can handle smaller holes down to 0.006”

1.7.3. The laser drill alignment target should **NOT** be used as the **MAIN** front to back alignment target. Use the front to back alignment target in section 6 instead.

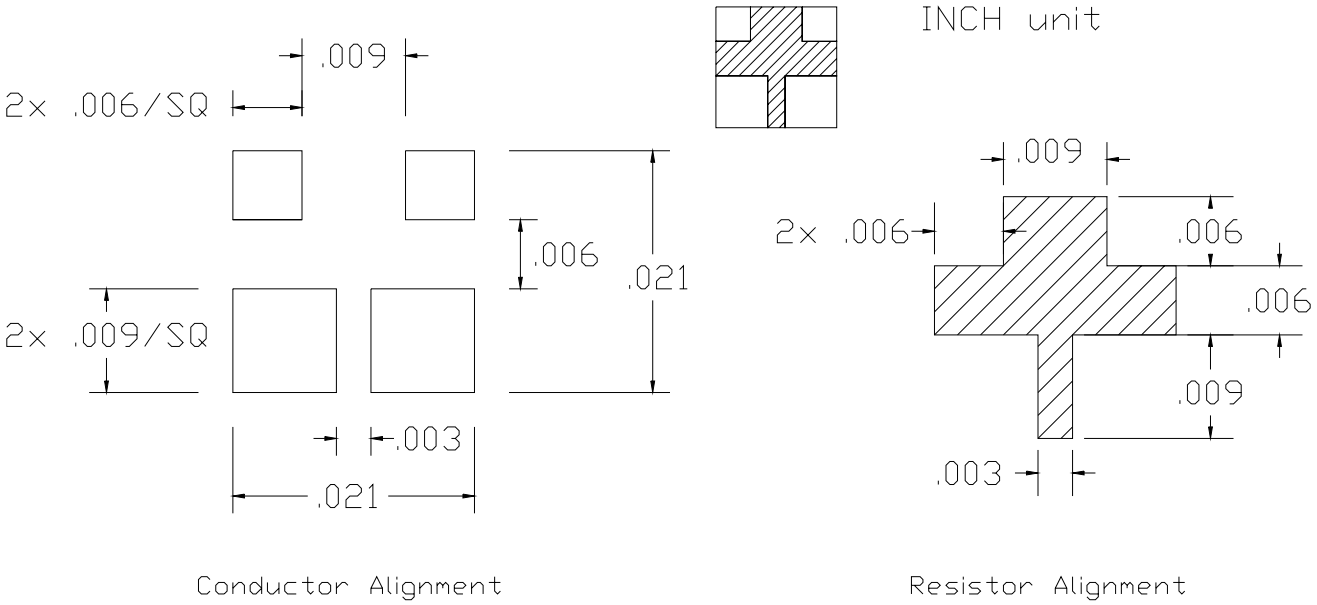
NOTES: NEVER design alignment target hole larger than the standard 0.010”. It is better using a smaller alignment target hole if critical alignment needed.



In a dark field mask, the cross laser drill alignment target has to be put in the middle of an open box to allow viewing substrate when aligning.



1.8. Conductor – Resistor Alignment Target:



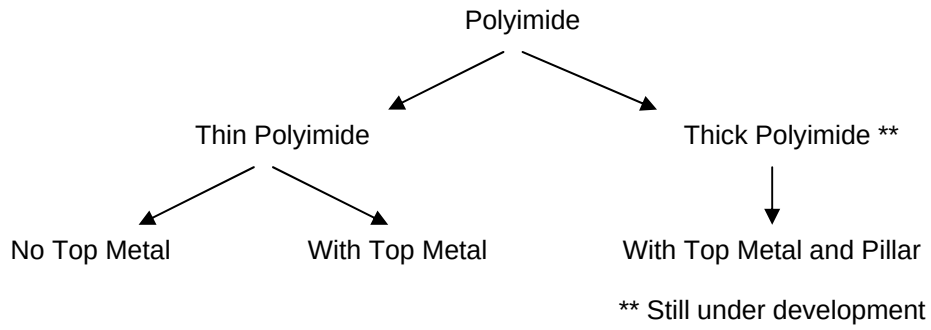
NOTE: The conductor – resistor alignment target can be scaled down to a smaller size if more precise alignment is needed.

2. Special Process – Polyimide Process

The mask type and size used for the polyimide layer are the same as those used for the conductor resistor layers. Polyimide acts in similar ways to those of negative photoresist. Any area that is covered by the opaque part of the mask will be made soluble by exposure to ultraviolet light. Those, which are not covered, will stay.

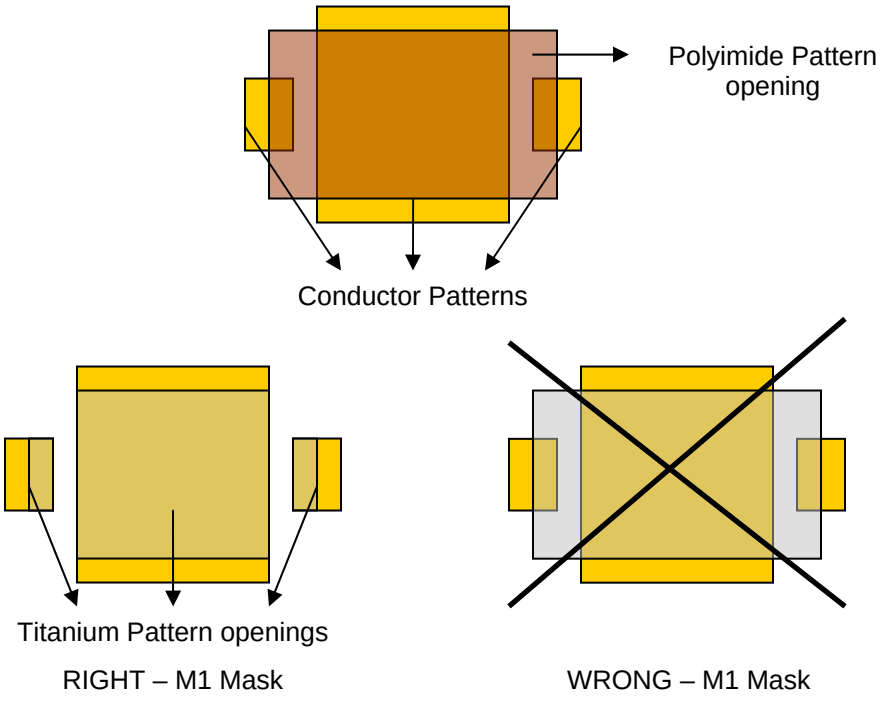
Different application of polyimide may require different polyimide thickness and also may be processed in a different way. Some of the applications may require another metal layer on the top of the polyimide layer; some of them may not. In certain design, another layer of mask for titanium metal might be required to help the adhesion of polyimide layer to the conductor pattern (gold layer) underneath it.

2.1. Process type



2.2. Mask Sequence:

2.2.1. The titanium mask– **M1**, if required, will be a **negative** image or a **dark** field mask. * **SEE DARK FIELD MASK NOTE.** The titanium patterns are usually the replica of the polyimide patterns that lies on top of conductor patterns **only**. The titanium patterns should **NOT** lies on top of ceramic or raw alumina substrate, in between two conductor patterns, since it might create some resistance. See below illustration.



The **open** areas will be:

a) The titanium traces

b) An open window with the top metal layer alignment target centered (T-shaped target). The top metal layer alignment target is used twice, first for the titanium layer alignment, second for the top metal alignment.

2.2.2. The polyimide mask –**P1** will be a **negative** image or a **dark** field mask. * **SEE DARK FIELD MASK NOTE**

The **open** areas will be:

c) The polyimide traces

d) An open window with the polyimide alignment target centered (P-shaped target).

2.2.3. The top metal mask – **T1** (if applicable) will be a **negative** image or a **dark** field mask. * **SEE DARK FIELD MASK NOTE**

The **open** areas will be:

a) The top metal layer traces

b) An open window with the top metal layer alignment target centered (T-shape target)

2.2.4. The top metal contact mask (**only** applicable for the **thick** polyimide **with top metal** layer) will be a **negative** image or a **dark** field mask. * **SEE DARK FIELD MASK NOTE**

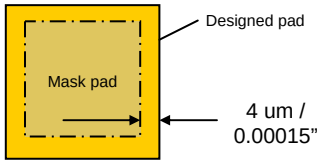
The **open** areas will be:

a) The top metal layer traces

b) An open window with a pillar alignment target centered

2.3. Polyimide Etch Factor

The following etch factor have to be applied:

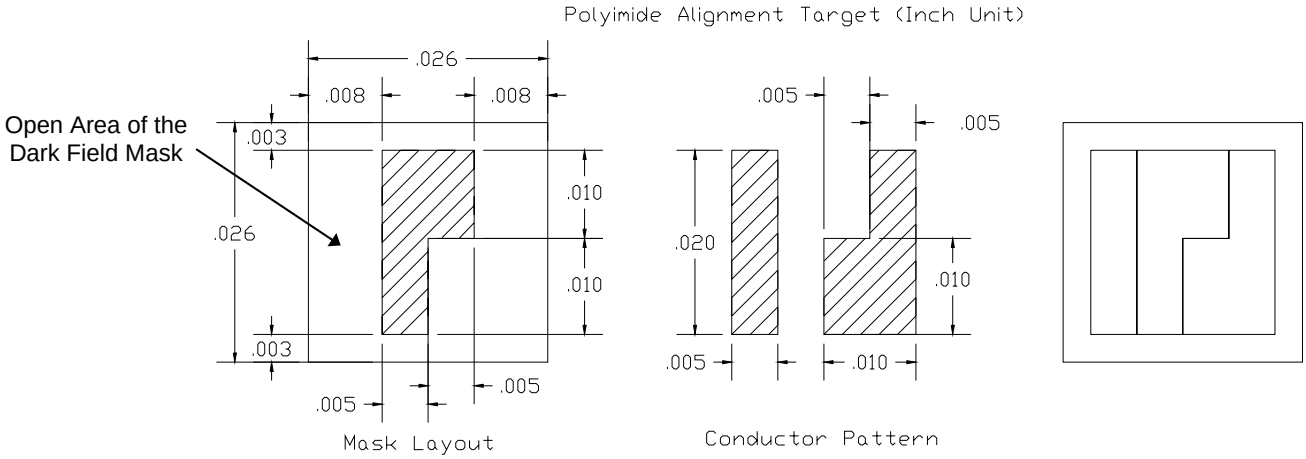


POLYIMIDE

+ 8 um / 0.0003”
Mask pad is **SMALLER** than the designed pad

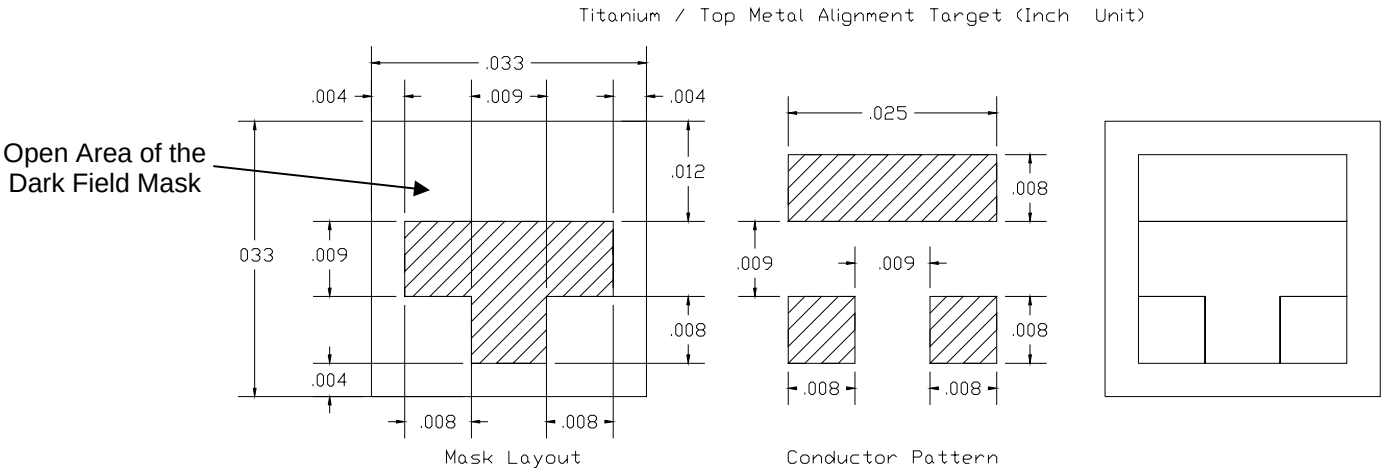
2.4. Polyimide Alignment Target

The polyimide alignment target is centered in an open window of the dark field mask. It aligns the polyimide layer (P1) to the conductor layer (C1 or PP1) behind it. The open window will help when looking for the target when aligning. Make sure to have the conductor alignment target on the conductor layer for aligning.



2.5. Top Metal Alignment Target

Both the top metal layer alignment (T1) and the titanium layer (M1) alignment are using the same target, which is a T-shaped target, centered in an open window of the dark field mask. It aligns both the top metal layer (T1) and the titanium layer (M1) to the bottom conductor layer (C1 or PP1). Make sure you have the other three patterns on the conductor layer mask for aligning.



2.6. Top Metal Contact Alignment Target (STILL UNDER DEVELOPMENT)

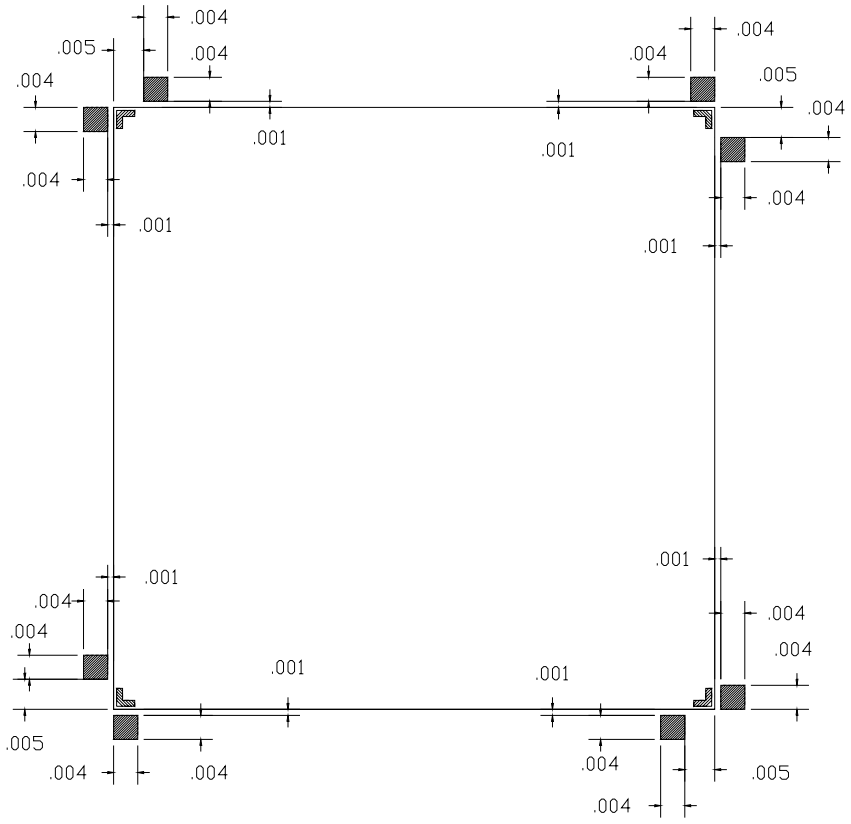
The Top Metal Contact alignment target is centered in an open window of the dark field mask. It aligns the top metal contact layer to the bottom conductor layer. Make sure to have the other patterns on the conductor layer. More information will come later.

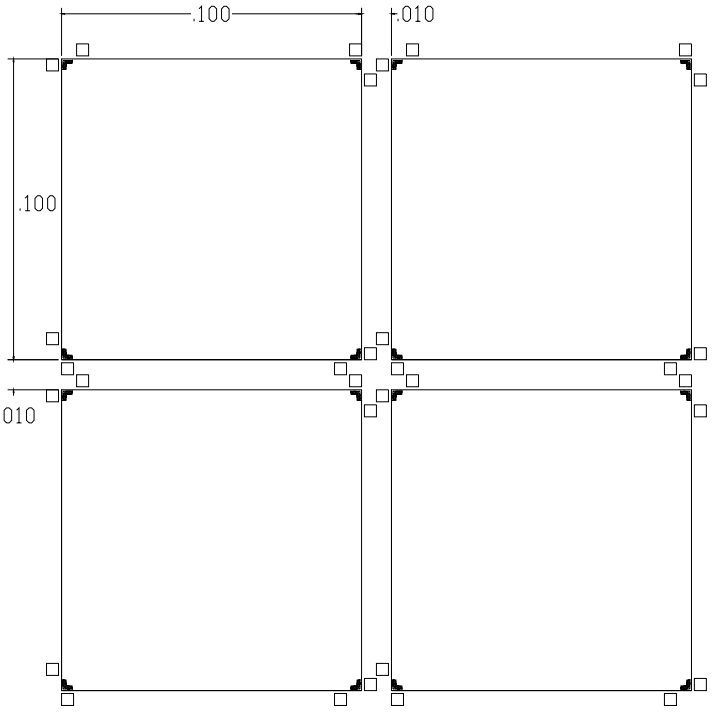
3. Cutting Targets:

The standard saw blade kerf is .010", but we also have a .020" one. If you have any slot designs that are located in the edge of the circuit, you need to use the 0.020" blade. There are two different cutting targets required: The first is the square ones located outside the circuit, in the dicing street. There are two squares located in each circuit corner. The second is the corner target inside the circuit, used as an indicator for the final inspector to check cutting result after dicing has been done. There should be one corner target in each circuit corner, if space is available. If not, there should be a minimum of two corner target in each circuit. All these cutting targets should be included in the artwork of the circuit front conductor mask (C1 or PP1) and have the exact dimensions, without etch factors. Its dimension is shown for inch and metric units, respectively.

NOTE: Use **0.26 mm** when converting the **0.010"** saw blade kerf from British to metric unit

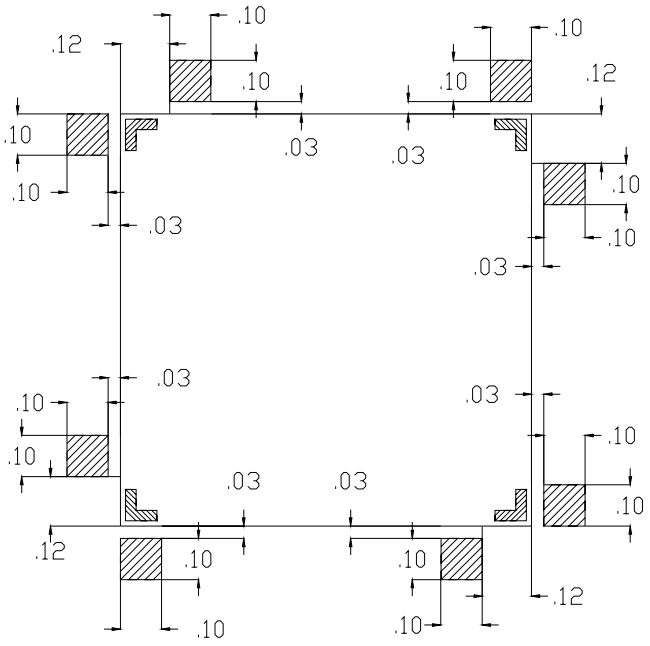
CUTTING TARGETS (INCH UNIT)

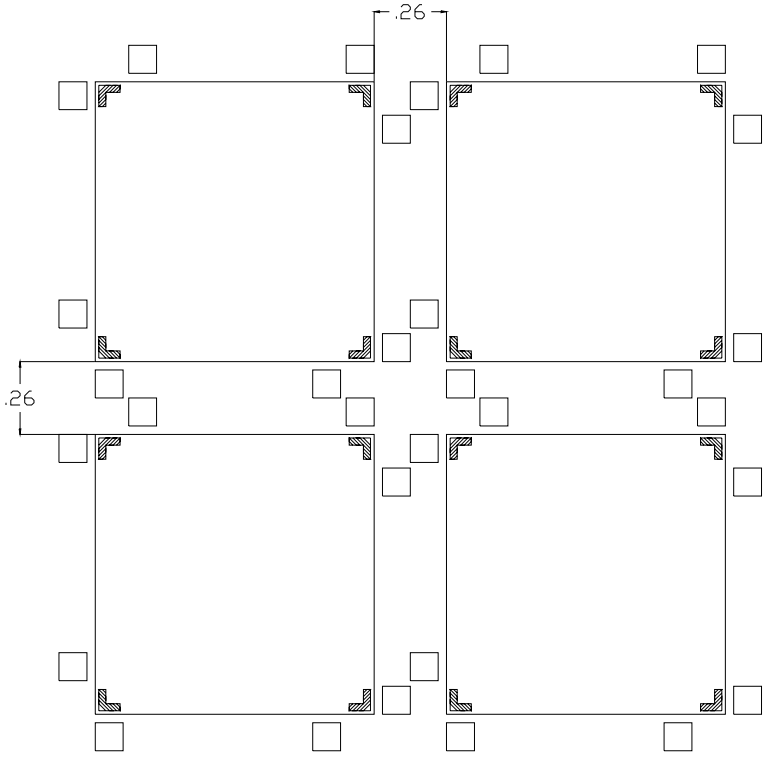




0.010" gap from circuit to circuit

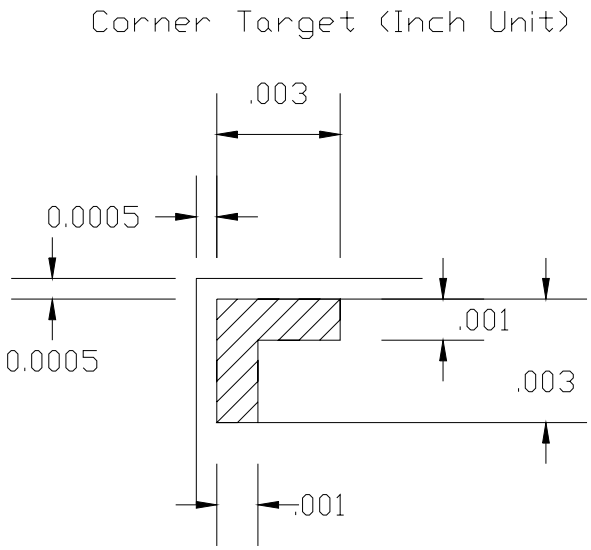
CUTTING TARGETS (METRIC UNIT)





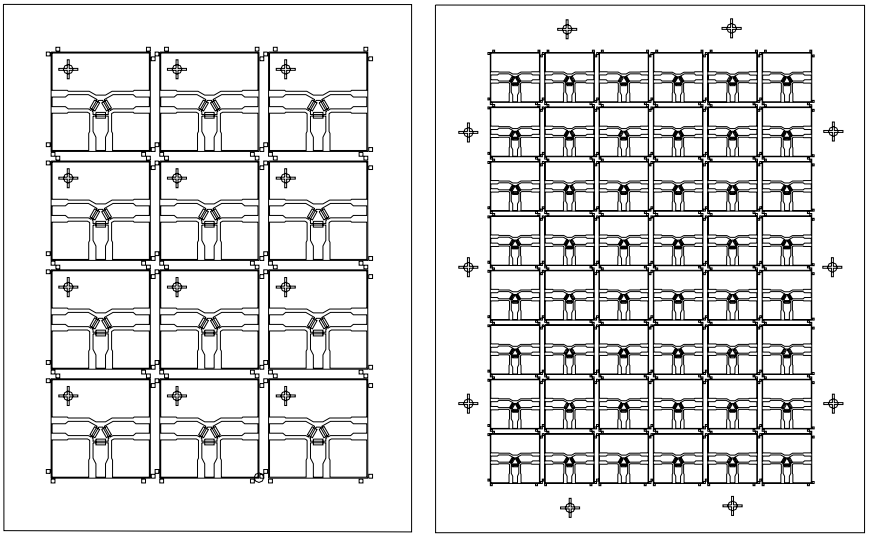
.26 mm gap from circuit to circuit

The following shows the dimension for the corner target inside the circuit. There should be one target in each circuit corner, if space is available. If not, there should be a minimum of two corner targets in each circuit. The



4. Step and repeat spacing:
   Should be the circuit dimension plus the saw blade kerf, either .010” or .020” on center.
   NOTE: Use **0.26 mm** when converting the **0.010”** saw blade kerf from British to metric unit

5. Laser drilled hole targets:
   The standard laser drill alignment hole target is .010” in diameter. If it is possible, it is preferred to have one alignment target in each circuit, rather than having them outside the circuit. Use outside alignment target only if space is not permitted.

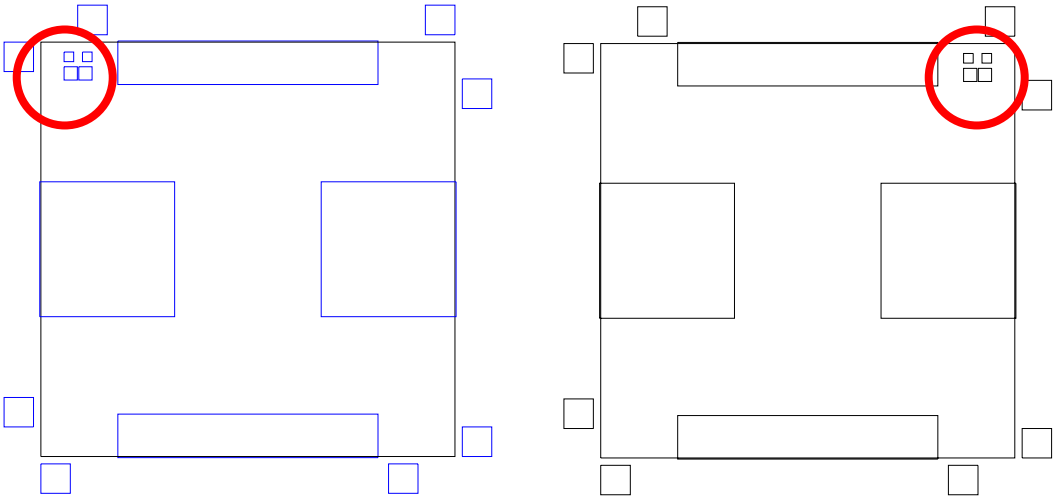


6. Front to back alignment target

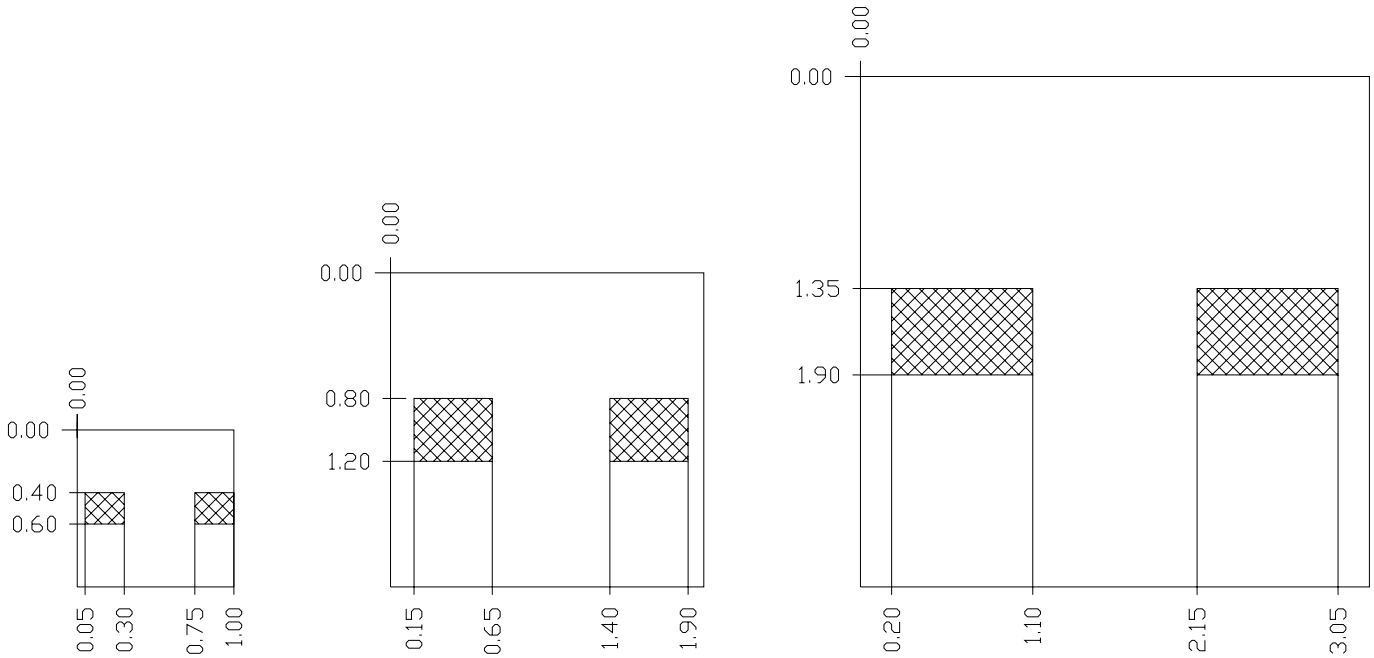
There are two different front-to-back alignment targets that are required:

a. The conductor pads on the conductor - resistor alignment target will be used as the **MAIN** front to back alignment target. There are two design rules when applying it:

- Both of the alignment targets, one on the front (C1 mask) and the one on the back (C2 mask) have to be identical to each other.
- They must have the same y location point and are mirror image to each other on the x direction. See diagram below:

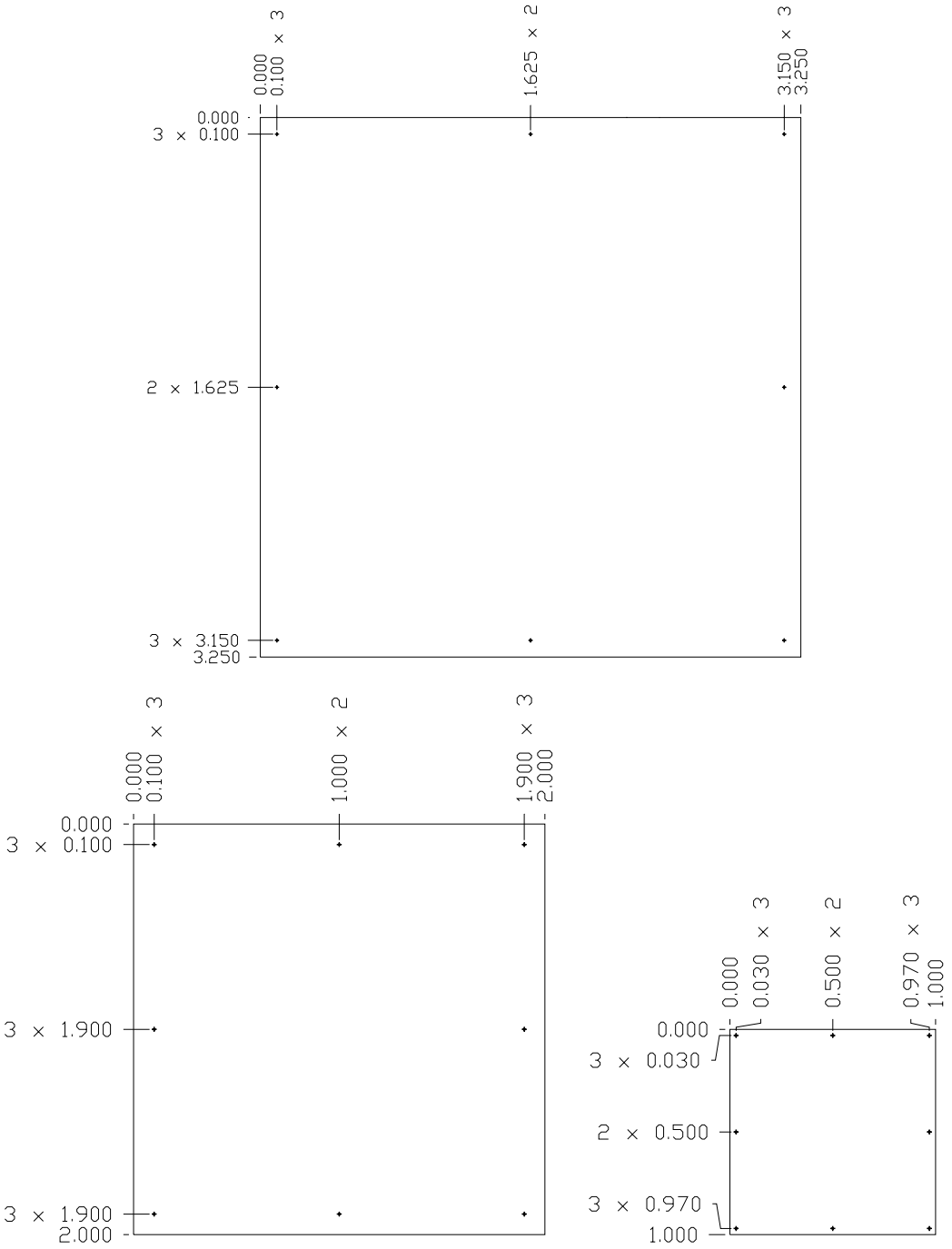


With the new aligner, front to back alignment can only be done if there are alignment targets located inside the hatched areas shown below for each different substrate size:



1” x 1” Substrate **2” x 2” Substrate** **3.25” x 3.25” Substrate**

b. The laser drill alignment target will be used as the **secondary** front to back alignment target. For substrates with vias, there is no additional laser drill alignment target required. For substrates without vias, the following laser drill alignment target should be added to both the front conductor layer (C1 or PP1) and the back conductor layer (C2 or PP2). These targets will be used in the case the new SUSS aligner is down and alignment have to be done using the old HTG aligner. These targets should be more precise compare to the old front-to-back substrate edge alignment target.



7. Fused Silica Substrate Exception

When using fused silica substrate and have gold layer on the back side, a **C2** mask is **required**, whether there is a backside pattern or not. The C2 mask must have the street lines between circuit to prevent peeling problem during the dicing process. Do **NOT** forget to include the front to back **alignment target** on the C2 mask.