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# 1. Scope

This document is intended to provide a guide to designers of thin film substrates. The guide is intended to document the substrate features that can be reliably and economically fabricated in Anritsu's Microwave Technology Center (MTC). In many cases, the limits stated herein represent features that have been successfully produced in the past, rather than a fundamental limit on the capabilities of a given process. As more definitive data is obtained on the processes, this procedure will be updated accordingly.

If a designer is able to produce a working design within the limits of this document, he can count on obtaining quality substrates. If the particular needs of a given design fall outside of these limits, the designer should discuss these needs with MTC personnel. It may be possible for the MTC to develop a new process or refine an existing process to achieve the desired result. It also may be decided that the existing processes can support the design even with low yields.

## 2. Applicable Documents

MTC-102 Guidelines for Mask Design

MTC-103 MTC Standard Notes

## 3. Order Requirements

MTC Engineering Request Form

-1 Drawing: Laser drill pattern (if applicable) \* See MTC-103

-2 Drawing: Metalization schemes \* See MTC-103

-3 Drawing: Finished Circuit Details \* See MTC-103

Design File (CAD File) is beneficial if the laser drill patterns are complex

## 4. Processing Overview

In order to produce thin film MIC circuits, the following steps are performed. These steps are somewhat simplified. Consult MTC if more detail is desired.

- Substrate Blanks are purchased
- Blanks are laser drilled (if applicable)
- Tantalum Nitride is sputtered onto the substrate (if applicable)
- Titanium Tungsten is sputtered onto the substrate
- Gold is sputtered and plated onto the substrate
- Photoresist is spun onto the substrate
- Photolithography transfers the pattern from the mask to the photoresist
- Gold is etched away where not desired to form the conductor patterns if using etch back process OR gold is plated in areas desired to form the conductor patterns if using pattern plate process
- Exposed Titanium Tungsten is etched away
- Photolithography transfers the pattern from the mask to the photoresist
- Tantalum Nitride is etched away where not desired to form resistors
- Resistors are heat treated to stabilize the values
- An adhesion layer of Titanium is deposited (capacitors and solder dams only)
- Polyimide is spun onto the substrate (capacitors and solder dams only)
- Polyimide is patterned and cured (capacitors and solder dams only)
- Top metal seed layer (Titanium – Titanium Tungsten -Gold) is deposited (capacitors only)
- Top metal is patterned by using pattern plate process (capacitors only)

- Resistors are either heat treated to final value or laser trimmed as specified
- Substrates are laser notched (post cut), if applicable
- Substrates are sawed into their final dimensions

## 5. Substrate Material

The standard substrate material used at Anritsu is alumina ( $Al_2O_3$ ), which is used in two forms: As Fired and Polished. As Fired has looser tolerances and a rougher surface finish, which makes it more difficult to hold tight tolerances on line widths and resistor values. Also, since the thickness tolerance is larger, even a line with a tight tolerance may not have the exact impedance desired. However, As-Fired material is cheaper and available in larger sizes, thus, if no critical features are required, it should be used. MTC reserves the right to use polished substrates in place of As-Fired at their discretion. On the other hand, As-Fired will not be used in place of polished without the designer's approval.

There are three other types of substrate material that MTC is capable of fabricating, alumina nitride, fused silica and polished sapphire. MTC may not have them on hand, but will assist on obtaining them. The following table shows the substrate material properties.

### Substrate Material Properties

Material	CLA Surface Roughness ( $\mu$ -inches)	Thickness Tolerance (inches)	Dissipation Factor at (1kHz) / 1MHz	Dielectric Constant (k)	Thermal Conductivity (W/mK)	Thermal Expansion ( $\mu$ "/inch/ °C)
As Fired 99.6% Alumina	A-side < 2 B-side < 3	Depend on thickness	(.0003) / .0001	9.9 $\pm$ 0.1	30	7.1
Polished 99.6% Alumina	< 0.5		.0001	9.9 $\pm$ 0.1	30	7.1
Aluminum Nitride *	8-24	$\pm$ 5%	0.001	8.6	170	4.6
Fused Silica *	7	$\pm$ 5%	.000015	3.8	1	.55
Polished Sapphire *	1.0	$\pm$ 5%	0.0086	11.5	N/A	5.3

\* Material Properties may vary depend on manufacturer and surface finish

### 5.1. Alumina As Fired

The following table shows all the different sizes and thicknesses of Alumina As-Fired substrates that we have on hand.

Thickness (inch)	Thickness Tolerance (inch)	Size (inch)	Part Number
.005	$\pm$ .0005	1.00 x 1.00	704-34
.010	$\pm$ .0005	1.00 x 1.00	704-35
		2.00 x 2.00	704-31
		3.25 x 3.25	704-61
.015	$\pm$ .00075	1.00 x 1.00	704-36
		2.00 x 2.00	704-32
		3.25 x 3.25	704-62
.025	$\pm$ .00125	1.00 x 1.00	704-37
		2.00 x 2.00	704-33
		3.25 x 3.25	704-63

## 5.2. Alumina Polished

The following table shows all the different sizes and thicknesses of Alumina Polished substrates that we have on hand.

Thickness (inch)	Thickness Tolerance (inch)	Size (inch)	Part Number
.003	± .0002	1.00 x 1.00	704-64*
.005	± .0002	1.00 x 1.00	704-46
		2.00 x 2.00	704-85
.006	± .0002	1.00 x 1.00	704-59*
.0075	± .0001	2.00 x 2.00	704-75*
.010	± .0001	2.00 x 2.00	704-43
	± .0002	3.25 x 3.25	704-86
.015	± .0002	2.00 x 2.00	704-44
		3.25 x 3.25	704-87
.025	± .0004	2.00 x 2.00	704-45
	± .0005	3.25 x 3.25	704-88

\* These substrates are available but are non-standard and should not be used unless absolutely necessary

## 5.3. Fused Silica

Thickness (inch)	Thickness Tolerance (inch)	Size (inch)	Part Number
.005	± .0002	1.00 x 1.00	704-69

## 5.4. Optimum Finished Substrate Dimensions

In order to minimize the cost per substrate, it is best if the substrate dimensions maximize the number of finished substrates per substrate blank. The width of the saw blade, known as saw kerf, is .26 mm. MTC requires a 3-mm border around the step and repeated pattern for handling. Therefore, the maximum size for a given number of rows or columns that can be fabricated on a substrate is calculated as follows:

$$MaximumDimension^* = \frac{[(Size\ of\ Substrate\ Blank) - (2 \times Border) - Saw\ Kerf(N - 1)]}{N}$$

\* Round down to nearest mm

Where Size of substrate blank  $\cong$  82.5 (for 3.25") or 50.8 (for 2.00") or 25.4 (for 1.00") mm

Border  $\cong$  3 mm (for 3.25" & 2.00") or 1.5 mm (for 1.00")

Saw Kerf  $\cong$  .26 mm (for 0.010") or .52 mm (for 0.020")

N is the number of rows and/or columns

### Maximum Number of Finished circuit

The following tables can be used to obtain the maximum number of finished circuit for 3.25" x 3.25", 2.00" x 2.00" and 1.00" x 1.00" substrate, respectively. If the finished substrate 'X' dimension is equal to or less than the dimension in the top row below and if your finished substrate 'Y' dimension is equal to or less than the dimension in the left column below,

then the number at the intersection of that row and column is the maximum number of finished circuits that can be yielded from the substrate blank.

### 3.25" x 3.25" Substrate Blank

	76.00	37.87	25.16	18.81	14.99	12.45	10.63	9.27	8.21	7.37	6.67	6.10	5.61	5.19
76.00	1	2	3	4	5	6	7	8	9	10	11	12	13	14
37.87	2	4	6	8	10	12	14	16	18	20	22	24	26	28
25.16	3	6	9	12	15	18	21	24	27	30	33	36	39	42
18.81	4	8	12	16	20	24	28	32	36	40	44	48	52	56
14.99	5	10	15	20	25	30	35	40	45	50	55	60	65	70
12.45	6	12	18	24	30	36	42	48	54	60	66	72	78	84
10.63	7	14	21	28	35	42	49	56	63	70	77	84	91	98
9.27	8	16	24	32	40	48	56	64	72	80	88	96	104	112
8.21	9	18	27	36	45	54	63	72	81	90	99	108	117	126
7.37	10	20	30	40	50	60	70	80	90	100	110	120	130	140
6.67	11	22	33	44	55	66	77	88	99	110	121	132	143	154
6.10	12	24	36	48	60	72	84	96	108	120	132	144	156	168
5.61	13	26	39	52	65	78	91	104	117	130	143	156	169	182
5.19	14	28	42	56	70	84	98	112	126	140	154	168	182	196

### 2.00" x 2.00" Substrate Blank

	44.00	21.87	14.49	10.81	8.59	7.12	6.06	5.27	4.66	4.17	3.76	3.43	3.14	2.90
44.00	1	2	3	4	5	6	7	8	9	10	11	12	13	14
21.87	2	4	6	8	10	12	14	16	18	20	22	24	26	28
14.49	3	6	9	12	15	18	21	24	27	30	33	36	39	42
10.81	4	8	12	16	20	24	28	32	36	40	44	48	52	56
8.59	5	10	15	20	25	30	35	40	45	50	55	60	65	70
7.12	6	12	18	24	30	36	42	48	54	60	66	72	78	84
6.06	7	14	21	28	35	42	49	56	63	70	77	84	91	98
5.27	8	16	24	32	40	48	56	64	72	80	88	96	104	112
4.66	9	18	27	36	45	54	63	72	81	90	99	108	117	126
4.17	10	20	30	40	50	60	70	80	90	100	110	120	130	140
3.76	11	22	33	44	55	66	77	88	99	110	121	132	143	154
3.43	12	24	36	48	60	72	84	96	108	120	132	144	156	168
3.14	13	26	39	52	65	78	91	104	117	130	143	156	169	182
2.90	14	28	42	56	70	84	98	112	126	140	154	168	182	196

### 1.00" x 1.00" Substrate Blank

In the case of 1.00" x 1.00" substrate blanks, MTC has reduced their border for handling from 3 mm to 1.5 mm. This allows for considerably more substrates per substrate blank; however, some of the substrates near the edge are likely to be damaged by handling.

	22.00	10.87	7.16	5.31	4.19	3.45	2.92	2.52	2.21	1.97	1.76	1.60	1.45	1.33
22.00	1	2	3	4	5	6	7	8	9	10	11	12	13	14
10.87	2	4	6	8	10	12	14	16	18	20	22	24	26	28
7.16	3	6	9	12	15	18	21	24	27	30	33	36	39	42
5.31	4	8	12	16	20	24	28	32	36	40	44	48	52	56
4.19	5	10	15	20	25	30	35	40	45	50	55	60	65	70
3.45	6	12	18	24	30	36	42	48	54	60	66	72	78	84
2.92	7	14	21	28	35	42	49	56	63	70	77	84	91	98
2.52	8	16	24	32	40	48	56	64	72	80	88	96	104	112
2.21	9	18	27	36	45	54	63	72	81	90	99	108	117	126
1.97	10	20	30	40	50	60	70	80	90	100	110	120	130	140
1.76	11	22	33	44	55	66	77	88	99	110	121	132	143	154
1.60	12	24	36	48	60	72	84	96	108	120	132	144	156	168
1.45	13	26	39	52	65	78	91	104	117	130	143	156	169	182
1.33	14	28	42	56	70	84	98	112	126	140	154	168	182	196

## 6. Metalization

The following table is the summary of MTC Metalization Specification.

Material Function	Types of Material	Thickness / Values
Resistor	Tantalum-Nitride (TaN)	Standard: 50 and 100 $\Omega$ / sq. Non standard: 10 – 100 $\Omega$ / sq.
Adhesion	Titanium-Tungsten (TiW)	500 Angstroms
Conductor	Gold (Au)	Standard: 2.5, 5.0 $\mu\text{m}$

The basic metalization scheme for thin film substrates contains Titanium – Tungsten (TiW) and Gold (Au). Tantalum Nitride (TaN) is only sputtered if there is a resistor design in the substrates. A range of sheet resistance is possible. Two values, 50  $\Omega$  / sq. and 100  $\Omega$  / sq. are the Anritsu standards. Resistors formed of this material require heat treating for stability. Generally, the Tantalum-Nitride is sputtered about 20% lower in sheet resistivity than the final desired value. Usually the designer does not need to worry about this process since only the final sheet resistivity is important. The exception occurs with the introduction of laser trimming, especially if there are laser and non-laser trimmed resistors on one substrate, more thought must be put into the design of the resistors. This will be discussed further in the resistor section of this guide. Titanium – Tungsten (TiW) is used as a diffusion layer, while gold is the standard conductor metal at Anritsu. The gold thickness standard is 2.5  $\mu\text{m}$ .

## 7. Conductor Patterns

### 7.1. Minimum Line Width

The thinnest line attainable is 10  $\mu\text{m}$  standard\* with a tolerance of  $\pm 2 \mu\text{m}$

### 7.2. Minimum Gap

The narrowest gap attainable is 10  $\mu\text{m}$  standard\* with a tolerance of  $\pm 2 \mu\text{m}$

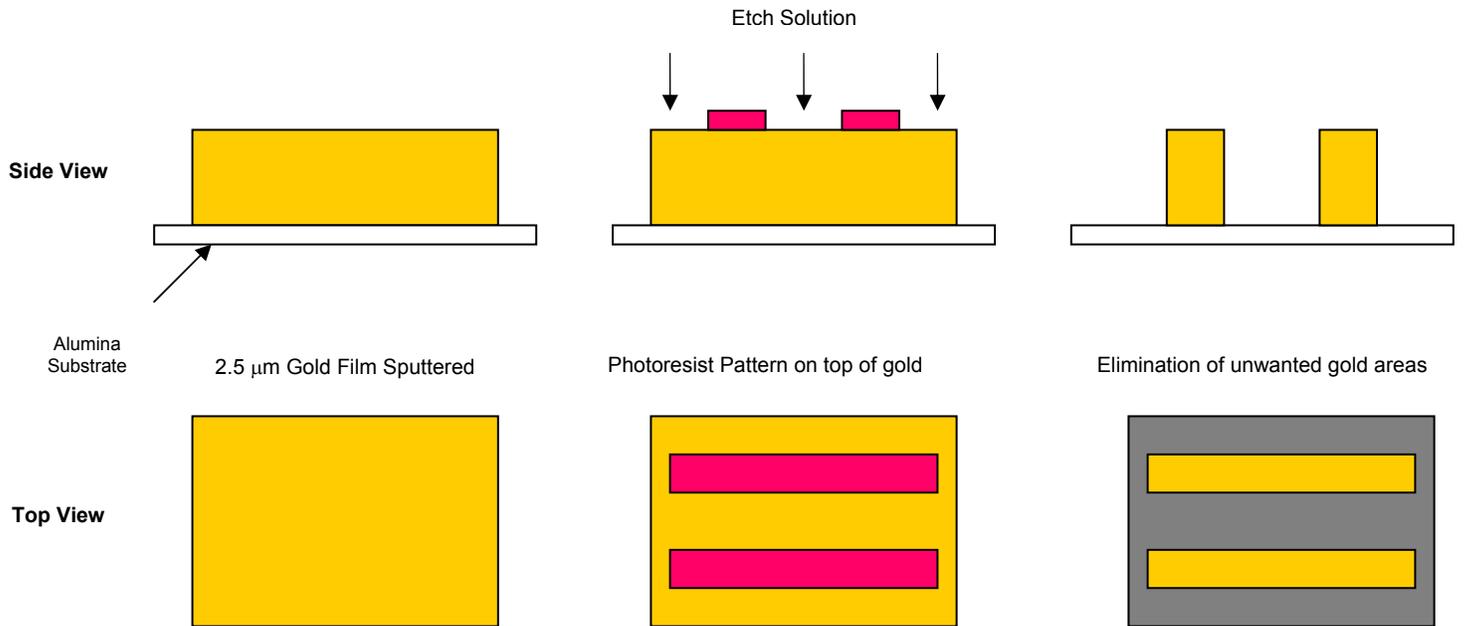
\*MTC will attempt to fabricate substrates with smaller line widths and / or narrower gaps with decreasing yields as the dimension get smaller. If these small dimensions are needed, make sure to order chrome on glass masks.

### 7.3. Fabrication Process

There are two different processes used to fabricate the conductor, the etch back process and the pattern plate process. The etch back process is currently the standard process used in MTC. It is easy to do, however, when the design involves numerous via holes and slots features, it would be better to use the pattern plate process. Pattern plate process has higher accuracy patterning capability and also reduces the material cost and labor. However, it will need an extra mask compared to the etch back process if the design includes via holes and slots.

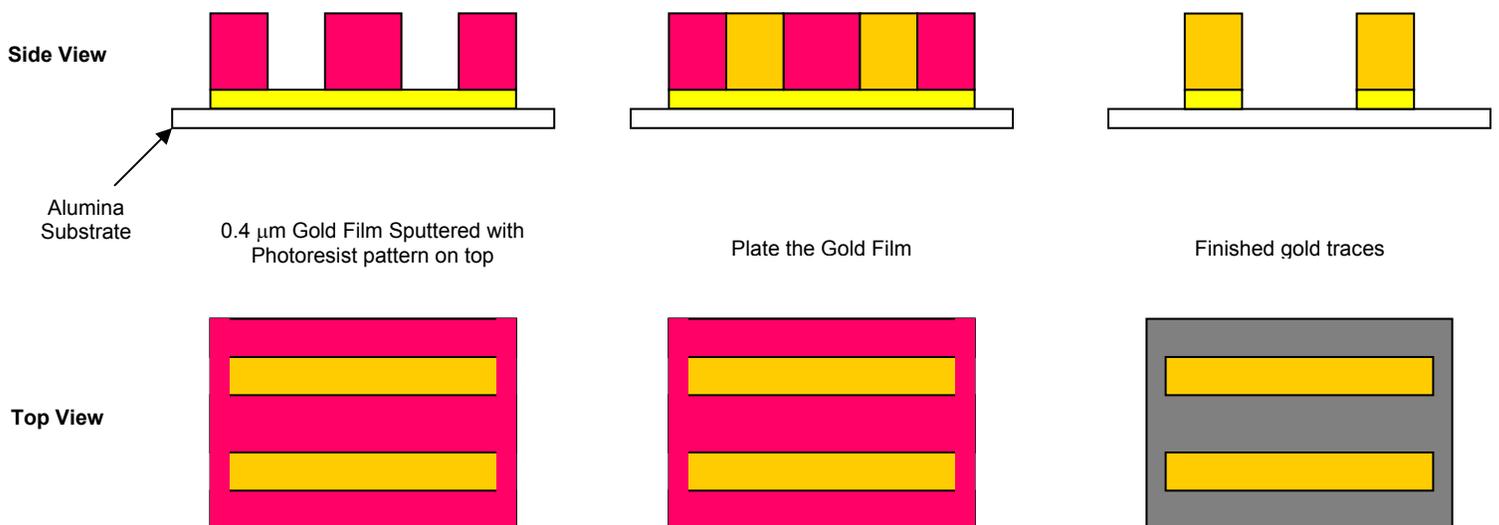
### 7.3.1. Etch Back Process

Etch back process forms the conductor pattern by selectively etching gold away from a substrate through a photoresist mask layer. The conductor pattern is protected by the photoresist during the etching process. The gold traces formed are slightly smaller, because of the existence of etch factor than the photoresist trace.



### 7.3.2. Pattern Plate Process

Pattern Plate process creates a pattern by selectively gold plating a substrate through a photoresist mask layer. The etch factor is smaller compare to the etch back process since the plating is constrained by the photoresist walls.



### 7.4. Etch Factor

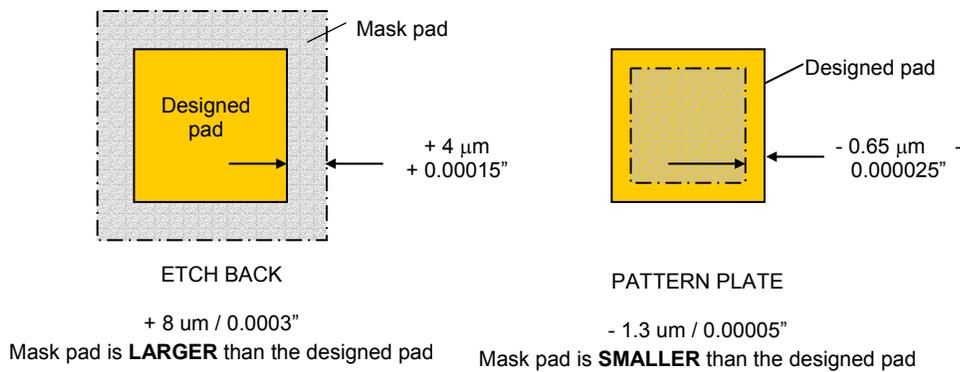
Since the two processes work on the opposite way to each other, different etch factor should also be applied. For the etch back process, lines become narrower and gaps become larger than the dimensions on the mask. For critical

dimension, an etch factor should therefore be designed into the artwork. A line will decrease by 8  $\mu\text{m}$  and a gap will increase by 8  $\mu\text{m}$ . For example, a Lange coupler with line widths of 30  $\mu\text{m}$  and gaps of 25  $\mu\text{m}$  are desired. The mask should be designed with line widths of 38  $\mu\text{m}$  and gaps of 17  $\mu\text{m}$  to achieve the desired dimensions.

On the opposite, for the pattern plate process, line become wider and gaps becomes narrower. In the example of Lange Coupler, the mask should be designed with line widths of 28.7  $\mu\text{m}$  and gaps of 26.3  $\mu\text{m}$  to achieve the desired dimensions. For resistors with critical tolerances and small physical size, this etch factor should also be applied to the gold conductors forming the gap which the resistor will bridge.

The following table shows both of the etch factor. Be careful with the difference sign of the etch factor. The diagram below the table will help explain the difference.

Type of process	Etch Factor (both sides)
Etch back	+ 8 $\mu\text{m}$ / 0.0003" / 0.3 mil
Pattern Plate	- 1.3 $\mu\text{m}$ / 0.00005" / 0.05 mil



## 7.5. Trace to Edge Circuit

During the substrate sawing process, there is a significant possibility that substrate metalization will peel if the saw goes through a metalized portion of the circuit. Therefore, a minimum of 0.03 mm should be left between the metal trace and the edge of the circuit. The preferred margin is 0.05 mm.

## 7.6. Avoid Acute Angles

In the mask creation process, the patterns are formed on the mask using rectangular flashes of light. Certain patterns, especially acute angles, require numerous flashes to form. This can result in over exposure and bleed out in these areas of the mask.

# 8. Resistor Patterns

## 8.1. Minimum Resistor Dimension

The smallest resistor dimension should be 0.050 mm.

## 8.2. Resistor Values

The resistors used at Anritsu are normally formed from one of two standard sheet resistivity, which are 50  $\Omega/\text{sq}$ . and 100  $\Omega/\text{sq}$ . The value of a resistor element is calculated as follows:

$$R = \frac{L \times R_s}{W}$$

Where L = Length of Resistor  
W = Width of Resistor  
Rs = Sheet Resistivity (either 50 or 100 Ω / square)

### 8.3. Small Critical Resistors

When the value of a physically small resistor is important, remember to apply the etch factor to the gold traces that form the ends of the resistor.

### 8.4. Resistor Accuracy

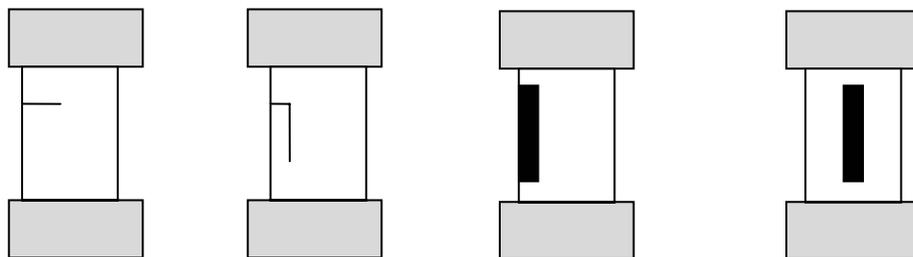
Resistors must be heat treated in order to be stable over time. Heat treating causes the value of a resistor to increase. Typically the resistive layer is sputtered on at approximately 80% of the final desired sheet resistivity and then the etched substrate is heat treated until a test resistor (or other resistor identified on the drawing as critical) is measured as being within 5% of its design value. For high accuracy resistors, etched resistors can be laser trimmed to tight tolerances after a minimum amount of heat treating has been performed.

Standard Resistor Accuracy – No Laser Trimming	
Test Resistor (or critical resistor)	5%
Other Resistors	15%

Laser Trimmed Resistors	
Standard	1%
Special	0.1%

### 8.5. Laser Trimming

There are four types of laser trimming patterns that can be specified: plunge, L, edge-trim and center trim. These are illustrated below:



Plunge

L

Edge Scan

Center Scan

#### 8.5.1. Plunge Cut

This cut is the quickest and easiest cut for the laser system to make. It is therefore the cheapest. Accuracy of 1% is achievable. The maximum allowable cut is 50% of the resistor width. This can seriously affect the power

handling capability of the resistor. Also, it does not result in a good RF match. This type of cut is best suited for reasonably high accuracy DC resistors with plenty of excess power handling capability.

### **8.5.2. L Cut**

This cut is similar to the plunge cut, but allows for higher accuracy. It is a little more expensive than the plunge cut. Accuracy of 0.1% is achievable. The first part of the cut is a plunge. This changes the resistor value quickly. Again, the maximum allowable plunge is 50% of the resistor width. This can seriously affect the power handling capability of the resistor. Also, it does not result in a good RF match. The perpendicular cut changes the resistor value very slowly, thus making high accuracy possible. This type of cut is best suited for very high accuracy DC resistors with plenty of excess power handling capability.

### **8.5.3. Edge-Trim**

This cut is made by trimming very slowly on the entire edge of a resistor. It is much more time consuming than the plunge or L cut. Accuracy of 0.1% is achievable. The same 50% of resistor width maximum cut applies. However, this cut generally results in much less narrowing of the resistor than the first two cuts. This means that the power handling ability of the resistor is less compromised. Also, RF performance is better than either of the first two cuts. This type of cut is best suited for very high accuracy DC resistors with more marginal power handling capability or RF resistors with moderate performance.

### **8.5.4. Center-Trim**

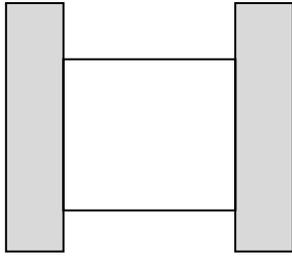
This cut is made by slowly trimming from the center of a resistor. It is the most time consuming trim performed and therefore the most expensive. The same 50% of resistor width maximum cut applies. However, this cut generally results in much less narrowing of the resistor than the first two cuts. This means that the power handling ability of the resistor is less compromised. Also, RF performance the best of any of the cuts. This type of cut is recommended for high performance RF resistors.

## **8.6. Combining Laser and Non-Laser Trimmed Resistors on One Substrate**

As laser trimming is time consuming and therefore expensive, it is often desirable to have critical resistors laser trimmed to tight tolerances while leaving the rest of the resistors untrimmed. In order for both types of resistors to achieve design values, the process must be adjusted slightly.

1. Design non-trimmed resistors for 90% of the nominal sheet resistivity (45 or 90  $\Omega$  / square)
2. Add a test resistor also designed to 90% of the nominal sheet resistivity
3. Design laser trimmed resistors for 100% of the nominal sheet resistivity
4. After etching, the substrate will be heat treated until the test resistor is within 5% of its design value.
5. Critical resistors are then laser trimmed to their final value.

### Example



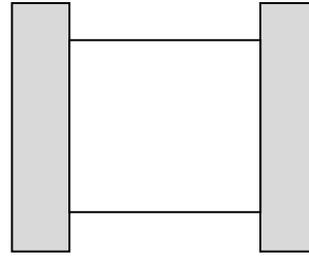
#### Non-Critical Resistor

Desired Value  $50 \Omega \pm 5\%$   
L = 50      W = 45

Before Heat Treating  
Value = 45  $\Omega$

After Heat Treating  
Value =  $50 \Omega \pm 5\%$

After Laser Trim  
Value = Unchanged



#### Critical Resistor

Desired Value  $50 \Omega \pm 0.5\%$   
L = 50      W = 50

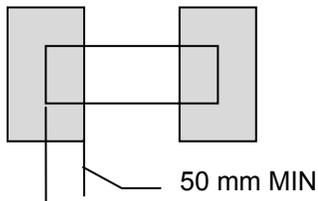
Before Heat Treating  
Value = 40.5  $\Omega$

After Heat Treating  
Value = 45

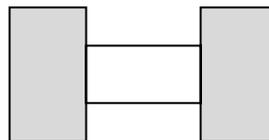
After Laser Trim  
Value =  $50 \Omega \pm 0.5\%$

## 9. Overlap of Resistors and Gold

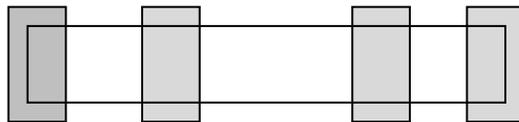
To avoid problems with small misalignment of the gold and resistor patterns, the resistor pattern on the resist mask should overlap the gold pattern by 0.05 mm minimum. Since this does not affect the final resistor in any way, overlap can be much bigger than 0.05 mm.



OK



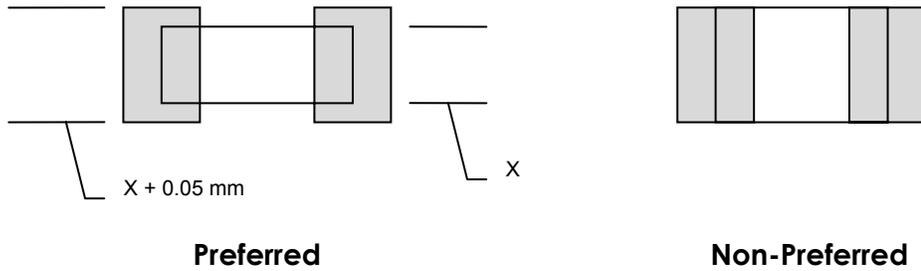
WRONG



OK

## 10. Gold Trace Larger than Resistor

To allow a margin for misalignment of resistors to conductor traces, it is preferred that the gold pads be 0.05 mm wider than the resistor.



## 11. Power Dissipation

No definitive studies have been performed to test the long-term reliability of the resistors built at Anritsu. Until these are performed we are using numbers that have been used commonly in the industry. Obviously, a lot of parameters will affect the power rating. If your circuit has poor heat sinking, tend to use the lower numbers; conversely, if you have a well heat sunk circuit, it is safer to use the higher numbers. The typical number, when applied to 25 mil micro strip circuits in a metal housing can be expected to change by less than 0.1% per year.

Most Conservative (MIL-SPEC for space applications)

50 Watts per square inch

Typical

400 Watts per square inch

Least Conservative

1200 Watts per square inch

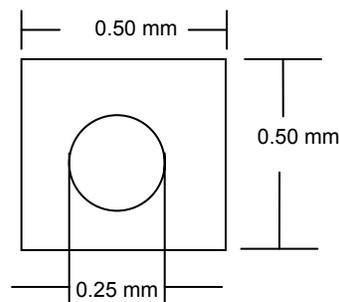
## 12. Vias, Slots and Laser Notch / Post Cut

### 12.1. Via Diameter

The standard via used at Anritsu is nominally 0.254 mm (.010") in diameter. The minimum via hole diameter that Anritsu is capable of doing is 0.152 (.006").

### 12.2. Pad Size for Vias

For etch back process, the edges of the conductor pad to the edges of the vias should be a minimum of 0.254 mm (0.005") via in all directions. For pattern plate process, smaller distance between the edges of the pad to the edge of the vias can be as small as 0.076 mm (0.003").



### 12.3. Distance from Edge of Via to Edge of Circuit

Vias placed near the edge of circuits are prone to cracking problems. Therefore, leave at least 0.010" or one substrate thickness distance, whichever bigger, between the edge of a via and the edge of the circuit.

#### 12.4. Distance between Vias

Vias placed close together are prone to cracking. Therefore, leave at least 0.010" or one time via diameter distance, whichever smaller, between via to via.

#### 12.5. Vias in a Line

Many Vias in a line are prone to cracking. Try to avoid many vias in a line in your design.

#### 12.6. Slots

MTC is capable of cutting different shape and sizes of slot and cut out, with or without metal. The minimum edge slot radius is .076 mm (.003"), which is the diameter of the laser beam itself. Consult MTC for feasibility.

### 13. Double Sided Circuits

Essentially, any circuit feature that can be realized on one side of a substrate can be realized on the back as well. It is easier if critical dimensions are limited to one side only. Circuits with complicated backside patterns should use polished substrate material.

#### 13.1. Front to Back Alignment

The alignment accuracy from the front to the back of a substrate is +/- 5 µm.

### 14. Step and Repeating and Alignment Marks

See MTC-DOC-02, the Guidelines for Mask Design for further information.

### 15. Polyimide

#### 15.1. General

Polyimide is a family of polymers, which are characterized by good mechanical properties, including fatigue resistance, excellent high temperature resistance or thermal stability, excellent chemical resistance and excellent electrical properties, particularly the dielectric strength. It is typically applied in liquid form, then thermally cured into a smooth, rigid, intractable polymeric film / structural layer. For most products, the film is patterned using photographic processes.

#### 15.2. Film Properties

The following are film properties of Durimide 7500 series, the polyimide brand used in MTC after it is cured at 350°C for an hour:

Tensile Strength	Mpa	215
Young's Modulus	Gpa	2.5
Tensile Elongation	%	85
Thermal Decomposition Temperature	°C	525
Coefficient of Thermal Expansion	ppm/°C	55
Coating Stress ( 100 Silicon)	Mpa	33
Dielectric Constant 1 MHz; 0% / 50% RH		3.2 / 3.3
Dissipation Factor 1 MHz; 0% / 50% RH		0.003 / 0.008

Dielectric Strength	V/ $\mu$ m	345
Moisture Absorption @ 50% RH	%	1.08
Density	g/cc	1.39
Refractive Index @ 633 nm		1.69

### 15.3. Applications

Currently, MTC is capable of making thin film capacitor, overlay coupler and solder dam using polyimide. For other different possible types of application and design, please consult MTC personnel.

#### 15.3.1. Capacitor

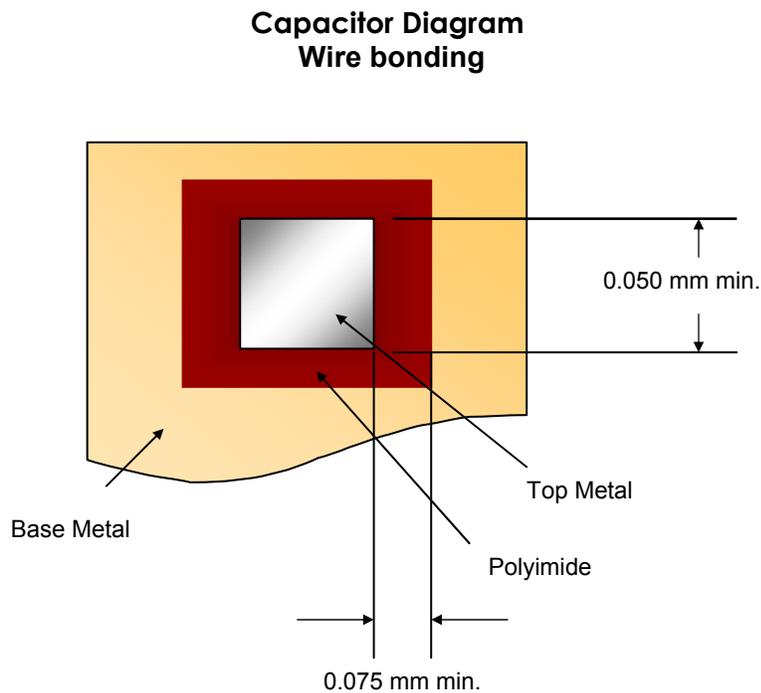
MTC thin film capacitor is in the pF range and has a breakdown voltage less than 100V. It can be fabricated using polyimide as a dielectric. Its unit capacitance is 7.1 pF/mm<sup>2</sup> based on a dielectric constant of 3.2 and a film thickness of 4.0  $\mu$ m. The tolerances will be 5% - 10% depending on size.

#### 15.3.2. Top Metal

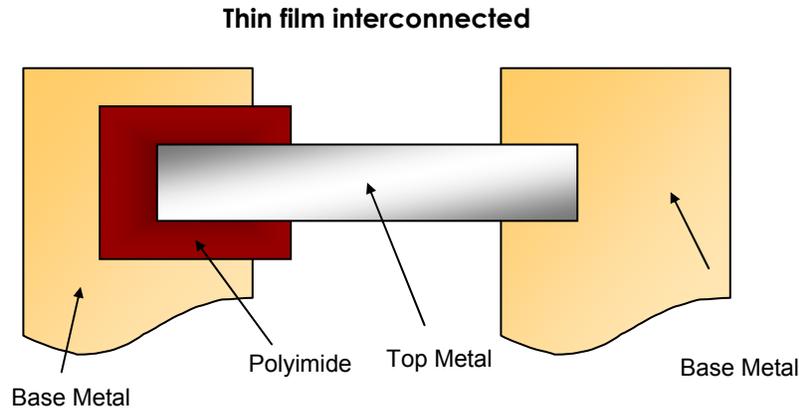
The top metal layer consists of sputtered Titanium (50 nm), Titanium Tungsten (50 nm) and electroplated gold (2.5 $\mu$ m).

#### 15.3.3. Connection

Connections can be made either by wire bonding or thin film connections. Minimum layout dimensions are shown below:

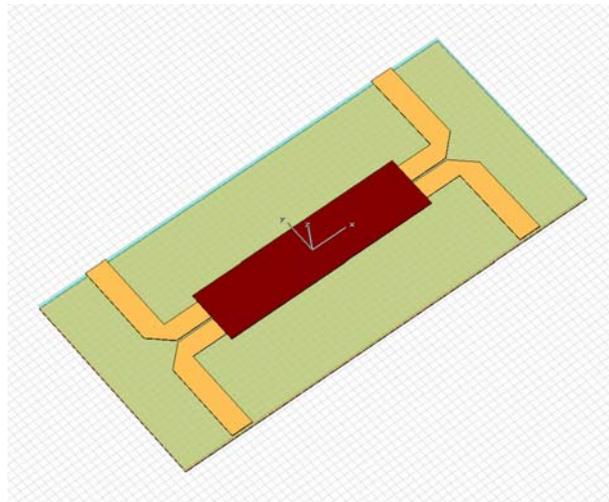


For wire bonding purposes, the minimum dimension for the top metal layer would be 0.1 mm x 0.1 mm. The distance from the polyimide edge to the top metal layer edge should be more than 0.08 mm. See above diagram.



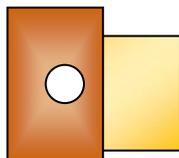
#### 15.4. Overlay Coupler

A thin layer of polyimide is fabricated on the top of the two closely spaced parallel lines to increase the coupling factor. This type of coupler can be used as a substitute for Lange coupler, with the advantages of higher performance, more simplified design and less sensitivity with line width between the gap of the coupler.



#### 15.5. Solder Dam

Various shapes of solder dams can be fabricated using polyimide. The purpose is to prevent the solder from flowing to unwanted areas. Polyimide has excellent chemical resistance, fluxes and cleaning solvents do not affect the cured polyimide. It also has excellent high temperature performance, thus it will withstand the 400°C reflow temperature. Sample layout can be seen as follows:



### 16. Sample Substrate Design

